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TITLE: JITTER REDUCING APPARATUS USING DIGITAL MODULATION TECHNIQUE

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JITTER REDUCING APPARATUS USING DIGITAL MODULATION TECHNIQUE

BACKGROUND OF THE INVENTION

1. Field of the Invention

[1] The present invention relates to an apparatus for reducing jitter occurring from a Synchronous Digital Hierarchy (SDH) network and, more particularly, to a jitter reducing apparatus using a digital modulation technique.

2. Background of the Related Art

[2] A digital communication network has a function, which existing analog networks lack, of synchronizing a clock frequency of every digital exchange within a network. In general, once synchronization between the connected digital exchanges is established, the digital transmission units are automatically maintained in synchronization. Such synchronization of digital exchanges within a digital network at the level of the whole communication network is called a synchronization plan or a network synchronization.

[3] Figure 1 is a schematic block diagram of a general synchronous system digital communication network. Digital exchange-1 includes a clock-1 and digital exchange-2 includes a clock-2. A trunk matching circuit accommodates a digital trunk line of the digital exchanges. Each digital trunk line includes an elastic store.

[4] If clock-1 is faster than clock-2, causing the writing speed in the elastic store of digital exchange-2 to exceed the reading speed, a data overflow occurs periodically in the elastic

store and results in a data loss. Conversely, a data underflow condition occurs in the elastic store of digital exchange-1, also causing a data loss.

[5] A short cycle of error of the clock frequency is absorbed by the elastic store, but, if the error of the clock frequency continues for a long time, a phenomenon occurs that a data loss repeatedly occurs due to the overflow or the underflow of the elastic store. No matter how high the stability of the clock inserted in the digital exchange is, an unstable component of the clock is introduced in a bit stream due to a physical variation of a transmission medium, which is called jitter.

[6] Figure 2 is a schematic block diagram showing the construction of a jitter reducing apparatus in accordance with the background art. A conventional jitter reducing apparatus includes a digital part and an analog part. The digital part includes an elastic store (ES) 1, a threshold level detector 2, a smooth read pattern generator 3, a Phase Locked Loop (PLL) store 4, and a phase comparator 5. The analog part is a PLL 6 consisting of Low Pass Filter (LPF) and a voltage controlled oscillator.

[7] ES 1 is a buffer for storing data inputted from the SDH network and has a storing structure of 8 bytes (width) * 32 (depth). The threshold level detector 2 compares an offset value of a WAD[4:0] signal and a RAD[4:0] signal of ES 1 and controls the smooth read pattern generator 3 based on the comparison. That is, the threshold level detector 2 obtains a difference value between the amount of data stored in ES 1 and the amount of data outputted from ES 1. If the amount of data stored in ES 1 is greater than the amount of data outputted, the threshold

level detector 2 controls the smooth read pattern generator 3 to output the data faster using the REN signal.

[8] While the PLL store 4 is reading a gapped data stored in ES 1, the smooth read pattern generator 3 changes a burst pattern of the gapped data to a smooth pattern having uniform timing, which is called a flattening function. PLL store 4 stores the data of ES 1, which has undergone the flattening process, and has a storing structure of 8 bytes (width) * 8 (depth).

[9] Phase comparator 5 detects a phase difference between a write clock frequency and a read clock frequency of the PLL store 4 and outputs it to the LPF of PLL 6. The LPF of the analog part removes a jitter component, which has moved to a radio frequency band, by a method for extracting only a low frequency component. The voltage controlled oscillator (VCO) controls the read clock frequency and maintains the locked state of PLL 6.

[10] A Plesiochronous Digital Hierarchy (PDH) signal flowing in from the SDH network is stored in ES 1. The PDH signal is pure PDH data (WE[7:0] & WEN) of which overhead and control data required for the SDH network have been already removed by the SDH Path Terminating unit.

[11] Data stored in ES 1 is read by the smooth read pattern generator 3. Data inputted to the ES 1 is of a burst pattern having an irregular timing, while data outputted from ES 1 is of a smooth pattern having an even timing distribution. The smooth read pattern generator 3 is controlled by the threshold level detector 2 so that the amount of data stored in ES 1 and the amount of data outputted from ES 1 can be constantly maintained.

[12] The data (RD[7.0] & REN) read by the smooth read pattern generator 3 is stored in the PLL store 4 and then a final PDH signal is restored by phase comparator 5 and PLL 6. The restored PDH signal is transmitted through a transmission line to a PDH transmission network.

[13] Phase comparator 5 measures a phase difference between the write clock frequency (an external reference clock frequency) and the read clock frequency (an internal clock frequency) created from the VCO. Then, a noise component of the measured value is removed and supplied to the VCO. The VCO controls the read clock frequency so the read clock frequency and the write clock frequency correspond to each other.

[14] In the background art apparatus, controlling the speed of reading data from ES 1 depends only on the offset comparison between the WAD[4:0] and the RAD [4:0] signals. Thus, it is difficult to effectively reduce jitter. As the PDH signal containing the jitter is transmitted to the network, it causes a data loss or an error.

[15] As a solution to such problems, the background art apparatus additionally includes an analog circuit (not shown) to reduce the jitter, which, however, causes an increase in cost.

SUMMARY OF THE INVENTION

[16] An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

[17] Therefore, an object of the present invention is to provide a jitter reducing apparatus using a digital modulation technique that is capable of solving the incomplete jitter removal problem. The jitter reducing apparatus is a digital device, thereby facilitating its implementation by a digital ASIC circuit.

[18] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein, there is provided a jitter reducing apparatus using a digital modulation technique including: an elastic store storing a data flowing in from an SDH network; a pattern generator controlling a data reading speed so as for the elastic store to maintain a certain data storing amount; a modulation sequencer generating a digital signal wave having a predetermined period and amplitude; and a phase level detector controlling the pattern generator by using the digital signal wave of the modulation sequencer.

[19] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[20] The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

[21] Figure 1 illustrates a schematic block diagram of a general digital communication network;

[22] Figure 2 illustrates a schematic block diagram of a jitter reducing apparatus of the background art;

[23] Figure 3 illustrates a schematic block diagram of a digital jitter reducing apparatus using a digital modulation technique in accordance with a preferred embodiment of the present invention; and

[24] Figure 4 illustrates a digital signal wave of a modulation sequencer in accordance with the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[25] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[26] Figure 3 is a schematic block diagram of a jitter reducing apparatus using a digital modulation technique in accordance with a preferred embodiment of the present invention. The digital jitter reducing apparatus includes a digital part and an analog part. The digital part includes an ES 1, a phase level detector 2a, a modulation sequencer 7, a pattern generator 3, a PLL store 4 and a phase comparator 5. The analog part is a PLL 6 consisting of an LPF and a voltage controlled oscillator.

[27] ES 1 is a buffer that stores data flowing in from the SDH network, having a size of 8 bytes (width) x 32 (depth). Modulation sequencer 7 generates a mode-value signal and a

mode-slope signal representing a modulation frequency having a certain period and amplitude and applies these signals to the phase level detector 2a. The phase level detector 2a compares an offset value of the WAD[4:0] and RAD[4:0] signals of ES 1 and controls the pattern generator 3 with the digital modulation frequency applied from the modulation sequencer 7. The operation of the phase level detector 2a is described more fully below.

[28] Phase level detector 2a receives four signals and controls the pattern generator 3 based on the four signals. The operation of the phase level detector 2a is as follows:

[29] In case that the input signal mode_slope is '0,' (WAD[4:0] + Mode_value[1:0]) - RAD[4:0].

[30] In case that the input signal mode_slope is '1,' (WAD[4:0] - Mode_value[1:0]) - RAD[4:0].

[31] The result value of the operation is in the range of 0~31. If the result value is between 0 and 15, the phase level detector 2a outputs '0' (H/L Req signal). If the result value is between 16 and 31, the phase level detector 2a outputs '1' (H/L Req signal), to control the pattern generator 3.

[32] When the pattern generator 3 receives '0,' it controls the data input/output speed between ES 1 and the PLL store 4 to be high. If, however, the pattern generator 3 receives '1,' it controls the input/output speed between ES 1 and the PLL store 4 to be low. In this manner, the pattern generator 3 controls the data stream speed as requested by the whole network.

[33] The phase level detector 2a includes an adder, subtracters and a comparator for the arithmetic operation. Whenever the mode_value[1:0] value is changed, the phase level

detector 2a performs the arithmetic operation to control the pattern generator 3.

[34] Thus, arithmetic operations are performed 16 times for one period (cycle) to control the pattern generator 3. This means that the amount of data inputted to and outputted from ES 1 can be quickly checked and the pattern generator 3 can be immediately controlled.

[35] The burst pattern of the incoming data (WD[7:0]) causes the jitter noise. Namely, when synchronized units receive and transmit data signals with each other, each data signal should maintain constant temporal intervals within the data stream. If the data signals have irregular temporal intervals, the data stream takes on a burst pattern. The pattern generator 3 changes such a burst pattern of the data stream into a smooth pattern under the control of the phase level detector 2a.

[36] While the PLL store 4 is reading a gapped data stored in ES 1, the pattern generator 3 changes a burst pattern of the gapped data to a smooth pattern having uniform timing. PLL store 4 stores the data of ES 1 that has undergone the flattening process, having a size of 8 bytes (width) x 8 (depth).

[37] Phase comparator 5 detects a phase difference between the write clock frequency and the read clock frequency of the PLL store 4 and outputs it to the LPF of PLL 6. The LPF of PLL 6 removes the jitter component, which has been band-passed to a high frequency, using a method for extracting only a low frequency component. The voltage controlled oscillator controls the read clock frequency to maintain the locked state of PLL 6.

[38] The operation of the digital jitter reducing apparatus of the present invention constructed as described above will now be explained. As for the PDH signal flowing in from

the SDH network, before it is inputted to a main apparatus, overhead and a control data which were required for the SDH network are all removed and only a pure PDH data (WD[7:0] & WEN) is stored in ES 1. Though the data written to ES 1 had the burst pattern with an irregular timing when stored to ES 1, it has the smooth pattern with uniform timing distribution, owing to the pattern generator 3, when read from ES 1.

[39] In this respect, the background art threshold level detector 2 controls the pattern generator 3 by sampling the difference value between the amount of data inputted to ES 1 and the amount of data outputted from ES 1. Comparatively, the phase level detector 2a of Figure 3 samples the difference value between the amount of data inputted to ES 1 and the amount of data outputted from ES 1 and digitally modulates the sampled difference signal using the digital signal wave of the modulation sequencer 7. Then, phase level detector 2a controls the pattern generator 3 with the resulting modulation value.

[40] In the above operational process, the phase level detector 2a is operated at constant time intervals upon receipt of a digital signal wave from the modulation sequencer. Pattern generator 3 also regularly performs a control operation of a pattern generation speed as well. The data (RD[7:0]&REN) read from ES 1 and stored in the PLL store 4, under the control of pattern generator 3, is then restored to the final PDH signal by phase comparator 5 and PLL 6. The restored PDH signal is transmitted through a transmission line to a PCH transmission network.

[41] Phase comparator 5 measures the write clock frequency and the read clock frequency of the PLL store 4 and outputs the measured value to the LPF of PLL 6. Then, the

LPF of PLL 6 removes only a noise component of the high frequency band from the inputted signal and outputs the signal to the VCO. Consequently, the VCO controls the read clock frequency so the read clock frequency and the write clock frequency correspond to each other, under the control of the phase comparator 5. This is required to perform synchronization between data transmission devices or networks by conforming the clock frequency of the network.

[42] Figure 4 is a diagram illustrating a digital signal wave form of a modulation sequencer in accordance with the present invention. The operation of the modulation sequencer 7 will now be described with reference to Figure 4.

[43] Modulation sequencer 7 receives an 8KHz frame signal and a 6.48MHz WCLK signal from an external SDH overhead processor. These signals have a time invariant phase, since they are synchronized with other systems in the network. The modulation sequencer 7 generates a mode_value [1:0] signal and a mode_slope signal according to the speed of the external clock. The mode_value [1:0] signal and the mode_slope signal have the forms shown in Figure 4.

[44] Modulation sequencer 7 outputs a mode-slope signal and a mode-value signal using a low and a high voltage level. Modulation sequencer 7 repeatedly outputs four signal values (00,01,10,11) indicative of an amplitude level of a digital signal wave, through a mode-value signal line, and outputs a signal indicative of a positive and a negative direction through a mode-slope signal line. In this manner, the modulation sequencer 7 implements a 16 divided-cycle digital signal wave having a constant amplitude and period. The positive portion of the

digital signal wave has a high level mode-slope signal, signifying the first 8 sections of the cycle, and the negative portion has a low level mode-slope signal, signifying the remaining 8 sections of the cycle. The modulation frequency of the modulation sequencer 7 has a 500 Hz bandwidth, achieved by dividing the 8KHz frame pulse into 16 sections.

[45] The value of the digital signal wave generated by the modulation sequencer 7 is increased or reduced by 1 as it is increased by stages from 0 to 3, for the first 4 sections of the frame pulse, and is reduced by stages reversely from 3 to 0 for the second 4 sections, during which the positive modulation (mode-slope = high level) is maintained. The value of the digital signal wave is decreased by stages from 0 to -3 for the third of the four sections and positively increased from -3 to 0 for the final four sections, forming a frame pulse of 16 sections. For the third and fourth of the four sections, the negative modulation (mode-slope = low level) is maintained, finishing one modulation period.

[46] As so far described, the jitter reducing apparatus using a digital modulation technique of the present invention has many advantages. That is, for example, by adding the modulation sequencer 7 generating a digital signal wave to the background art jitter reducing apparatus, the incomplete jitter removal problem of the background art is solved. In addition, since the jitter reducing apparatus is implemented solely by the digital circuit, the field Programmable Gate Array (FPGA) or the Application Specific Integrated Circuit (ASIC) can be easily implemented and applied thereby reduce the production cost.

[47] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to

other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.